Module Definition Form (MDF)

Module code: MOD002717	**Version:** 6 **Date Amended:** 07/Feb/2023

1. Module Title
Digital Systems Design with VHDL and FPGAs

2a. Module Leader
Sufian Yousef

2b. School
School of Engineering and the Built Environment

2c. Faculty
Faculty of Science and Engineering

3a. Level
7

3b. Module Type
Standard (fine graded)

4a. Credits
30

4b. Study Hours
300

5. Restrictions

Type	Module Code	Module Name	Condition
Pre-requisites:	None		
Co-requisites:	None		
Exclusions:	None		
Courses to which this module is restricted:	None		

LEARNING, TEACHING AND ASSESSMENT INFORMATION

6a. Module Description

The module provides a review of Digital Systems as well as their design philosophy in light of using modern Electronic Computer Aided Design (ECAD) tools for design, simulation and implementation of complex electronic circuits. The module introduces the modern top-down approach to VLSI circuit analysis, design and implementation techniques, aiming to shorten the design cycle and to manage an increased complexity. Programmable Logic Devices (PLDs), Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs) are briefly reviewed. VHDL (Very High Speed Integrated Circuit Hardware Description Language), a hardware description language largely used for holistic modelling of electronic systems and Integrated Circuit (IC) design, is presented and its syntax is discussed in detail, followed by practical design examples based on FPGA implementation. The thrust of the module is to develop Electronic System Design skills via theoretical analysis and case studies, which use industry standard software tools, bulding up on the previous knowledge in electronics. Every practising electronics engineer needs to have a strong working knowledge of VHDL design. Together with FPGAs, these two components of an electronics engineer's training are essential in order to design microelectronic systems largely based on this technology.

6b. Outline Content

- Design Flow and the role of Electronic Design Automation (EDA) tools and techniques in VLSI design. Top-down approach to circuit analysis, design and implementation techniques - FPGAs: *PLDs, ASIC and FPGA definitions; FPGA Architectures *Design routes for ASICs/FPGAs, versus economic factors, volumes, time-scales. *FPGA and ASIC Design; Programming *Xilinx and Altera Products; Product Selection - VHDL Design: *Fundamental Concepts; Basic Modelling Constructs; Design Units. Libraries. *VHDL Simulation & Delta ordering; Data Types and Operations; *Structural vs Behavioural Design; Sequential Statements; Parallel Statements; *Subroutines; Procedures and Functions. *Standard Packages; Files and I/O; *Design for Synthesis using VHDL. Good design practice. Design for test. - Case studies of VHDL design using FPGAs; industrial applications.

6c. Key Texts/Literature

The reading list to support this module is available at: https://readinglists.aru.ac.uk/

6d. Specialist Learning Resources

Electronics Laboratory equipped with appropriate instrumentation for VHDL design/development and FPGA programming. Electronic Design Automation software package and a range of FPGA development boards.

7. Learning Outcomes (threshold standards)		
No.	**Type**	**On successful completion of this module the student will be expected to be able to:**
1	Knowledge and Understanding	Demonstrate advanced knowledge of modern VLSI design techniques, and be able to critically evaluate and appropriately select ASIC/FPGA design and implementation routes in a top down approach.
2	Knowledge and Understanding	Perform in-depth analysis of design requirements and convert a set of specifications into a working product using state-of-the art design toolsand techniques, having gained a working proficiency of VHDL programming.
3	Knowledge and Understanding	Critically evaluate and select appropriate VHDL syntax, library procedures / functions and construct a set of test vectors to prove the operational performance of a design.
4	Intellectual, practical, affective and transferrable skills	Selectively decide on the appropriate FPGA for the task in hand, matching design concept complexity to physical devices, through the optimal use of VHDL based industry standard CAD tools in a hierarchical approach.
5	Intellectual, practical, affective and transferrable skills	Conceptually design, develop and implement sample electronic systems / subsystems, simulate/evaluate their functionality and validate their choicethrough timing analysis and experimental testing.
6	Intellectual, practical, affective and transferrable skills	Determine the range of operational frequencies for an FPGA device and specify its limitations, while dealing with clock skews / multi-clock systems.

8a. Module Occurrence to which this MDF Refers				
Year	**Occurrence**	**Period**	**Location**	**Mode of Delivery**
2024/5	ZZF	Template For Face To Face Learning Delivery		Face to Face

8b. Learning Activities for the above Module Occurrence			
Learning Activities	**Hours**	**Learning Outcomes**	**Details of Duration, frequency and other comments**
Lectures	24	1-6	Lectures every week: 2 h x 12 weeks
Other teacher managed learning	36	1-6	Practical lab/seminar work 3 hr x 12 weeks
Student managed learning	240	1-6	8 hr x 12 weeks = 96 hours spent working on Laboratory exercises; remaining time to be spent on library textbook/journal research and individual study.
TOTAL:	300		

9. Assessment for the above Module Occurrence					
Assessment No.	**Assessment Method**	**Learning Outcomes**	**Weighting (%)**	**Fine Grade or Pass/Fail**	**Qualifying Mark (%)**
010	Practical	3-6	70 (%)	Fine Grade	40 (%)
Coursework maximum 4000 Word Equivalent maps to Engineering Council Learning Outcomes M2, M7					
Assessment No.	**Assessment Method**	**Learning Outcomes**	**Weighting (%)**	**Fine Grade or Pass/Fail**	**Qualifying Mark (%)**
011	Coursework	1-2	30 (%)	Fine Grade	40 (%)
In class test 1 hour maps to Engineering Council Learning Outcome M1					

In order to pass this module, students are required to achieve an overall mark of 40% (for modules at levels 3, 4, 5 and 6) or 50% (for modules at level 7*).

In addition, students are required to:
(a) achieve the qualifying mark for each element of fine graded assessment as specified above
(b) pass any pass/fail elements

[* the pass mark of 50% applies for all module occurrences from the academic year 2024/25 – see Section 3a of this MDF to check the level of the module and Section 8a of this MDF to check the academic year]